The Optoelectronic Processing Unit (OPU)
A Bidirectional Architectural Primitive for Optical-Native Systems

Eric Li
Founder & Chief Architect, PhotonWeave

Executive Summary

As artificial intelligence and high-performance computing systems scale, electrical interconnects increasingly constrain bandwidth, power, and system complexity. Optoelectronic interconnects offer compelling advantages, but realizing their full potential requires architectural change, not incremental attachment to electrical-centric designs.

PhotonWeave introduces the Optoelectronic Processing Unit (OPU), a bidirectional architectural primitive that defines the boundary between digital system fabrics and optoelectronic interconnects. Complementary OPU-TX and OPU-RX units respectively generate and terminate spatial optoelectronic signals, consolidating optoelectronic modulation, detection, aggregation, and conditioning into dedicated processing units. By decoupling optoelectronic fabric handling from compute silicon, OPU enables optoelectronic-native scale-up architectures with higher bandwidth density, lower energy per bit, and greater system modularity.

Practicality and System Integration

While introducing a new architectural primitive may appear complex at first glance, the Optoelectronic Processing Unit is explicitly designed to integrate into existing digital system fabrics in a practical, incremental manner. OPU does not require changes to compute architectures, programming models, or system software. Instead, it consolidates optoelectronic functions that already exist in fragmented form—drivers, modulators, detectors, and conditioning—into a dedicated, physically proximate interface.

By aligning with mature 3DIC packaging flows and well-understood digital interfaces, OPU acknowledges the realities of manufacturing, yield, power delivery, and system bring-up. Its purpose is not to add complexity, but to remove it—by relocating optoelectronic handling from ad hoc system integrations into a clean, reusable architectural boundary.

Physical Integration via 3DIC Bonding

From a physical integration perspective, OPU-TX and OPU-RX are intended to be integrated using true 3DIC die-to-die bonding, rather than 2.5D interposer-based approaches commonly associated with HBM. Architecturally, this is closer to modern designs where compute dies are vertically bonded to dedicated I/O or interface dies at fine pitch.

In this model, OPU functions as a specialized optoelectronic interface die that is tightly bonded to the host ASIC through advanced 3D integration. This approach enables high bandwidth density, low latency, and efficient power delivery while preserving a clear

architectural separation between compute logic and optoelectronic fabric handling.

The emergence of mature 3DIC packaging technologies makes this integration practical today. In that sense, OPU is born at an inflection point where advanced packaging transitions from a niche capability to a mainstream system enabler.

1. The Limits of Electrical Scale-Up

Modern accelerators depend on massive scale-up bandwidth to support model parallelism, memory sharing, and distributed workloads. As bandwidth requirements grow into the multi-terabit-per-second regime, electrical interconnects encounter fundamental challenges. Power per bit rises sharply with signaling speed and reach, signal integrity margins shrink, thermal density increases, and system complexity grows due to retimers, equalization, and routing constraints.

2. The Need for Optoelectronic-Native Architectures

Optoelectronic interconnects offer distance-independent bandwidth scaling, lower energy per bit at high throughput, and immunity to electrical channel impairments. However, simply attaching optics to electrically optimized systems does not fully unlock these benefits. Optoelectronic interconnects must be integrated as first-class architectural elements rather than treated as peripheral extensions.

3. Defining the Optoelectronic Processing Unit (OPU)

The Optoelectronic Processing Unit (OPU) is a specialized silicon device that performs optoelectronic signal generation, detection, aggregation, and termination for high-bandwidth digital fabrics. Rather than embedding optoelectronic functions directly into compute silicon, the OPU provides a dedicated interface between digital systems and optoelectronic fabrics.

OPU is inherently bidirectional and consists of complementary transmit and receive roles:
• OPU-TX generates, modulates, and spatially organizes optoelectronic signals originating from the digital domain.
• OPU-RX terminates optoelectronic signals and presents them back to the digital system.

Together, OPU-TX and OPU-RX define a symmetric architectural boundary between compute systems and optoelectronic fabrics.

4. OPU as an Architectural Primitive

System architectures have historically evolved through the introduction of specialized processing units to manage growing complexity, including GPUs for parallel computation and DPUs for data movement. The OPU extends this progression into the optical domain.

By separating optoelectronic processing from compute logic, the OPU allows compute

silicon to focus on computation while OPUs handle optoelectronic fabric interaction. This separation improves scalability, power efficiency, and architectural flexibility.

5. OPU-Based Scale-Up Systems

In OPU-based systems, high-bandwidth digital fabrics terminate at OPU-TX and OPU-RX units rather than directly at compute cores. Optoelectronic links originate and terminate at the OPU, enabling scale-up bandwidth to increase without proportional growth in electrical I/O power or complexity. As a result, system fabrics become optoelectronic -native rather than electrically constrained.

6. Power, Bandwidth, and Modularity Advantages

By consolidating optoelectronic functions within a dedicated processing unit and eliminating long-reach electrical signaling, OPU-based architectures achieve lower system-level energy per bit, reduced thermal load on compute silicon, and higher aggregate bandwidth density. Architectural modularity allows optoelectronic technology to evolve independently of compute silicon, enabling long-term system evolution without rigid integration constraints.

7. Implications for Fabrics and Systems

OPU-based architectures enable optoelectronic -native fabrics with higher radix, flatter topologies, and reduced system complexity. As bandwidth demands continue to grow, such architectures provide a scalable foundation for future compute, memory, and networking systems.

8. Conclusion

The Optoelectronic Processing Unit represents a fundamental shift in how optoelectronic interconnects are integrated into high-performance systems. By defining a bidirectional, modular boundary between digital fabrics and optoelectronic interconnects, OPU enables scalable, power-efficient, and future-proof optoelectronic-native architectures.

About PhotonWeave

PhotonWeave develops optoelectronic-native system architectures that redefine how compute, memory, and communication scale. Through architectural primitives such as the Optoelectronic Processing Unit, PhotonWeave enables next-generation AI and HPC systems designed around first principles of physics and system architecture.

Eric Li is the founder of PhotonWeave, where he focuses on optical-native system architectures for next-generation AI and HPC platforms.